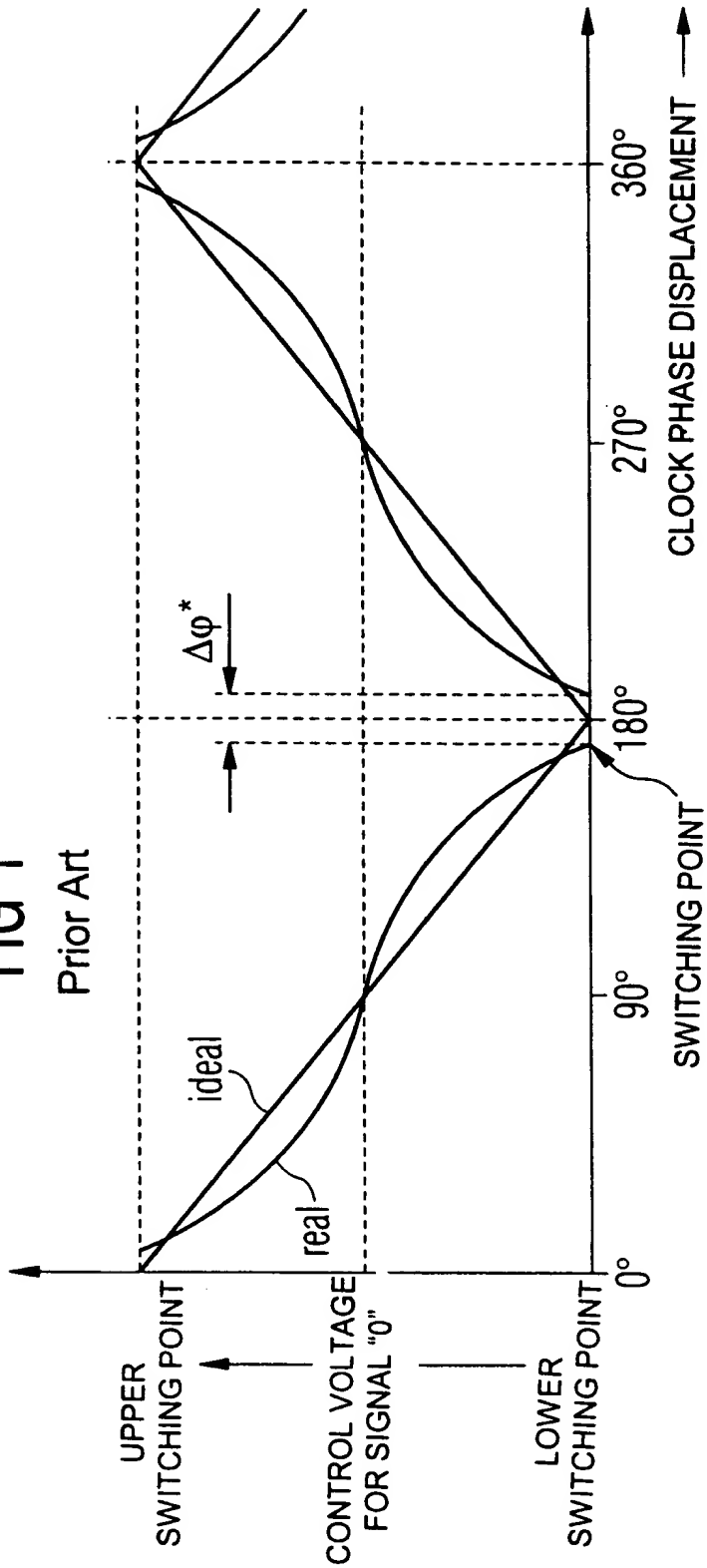
FIG 1
Prior Art



*) Δφ is a phase jump which occurs when the delay generator is changed over.

FIG 2

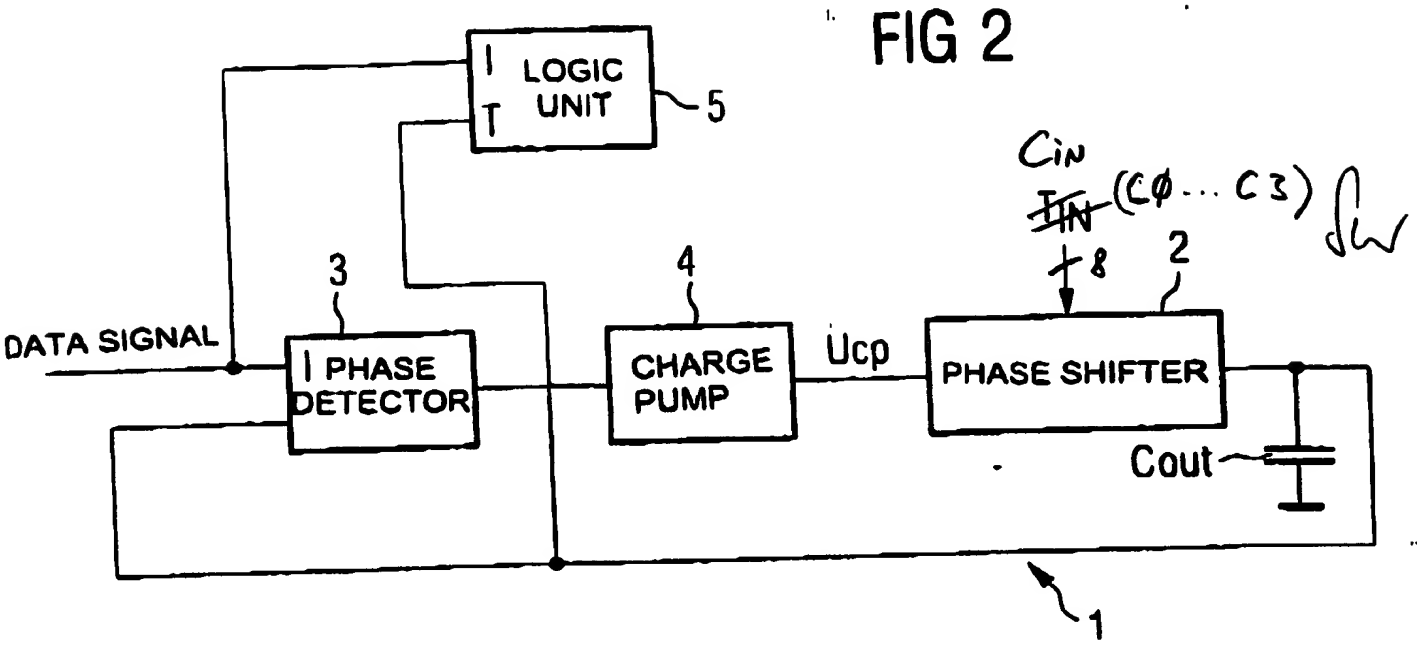
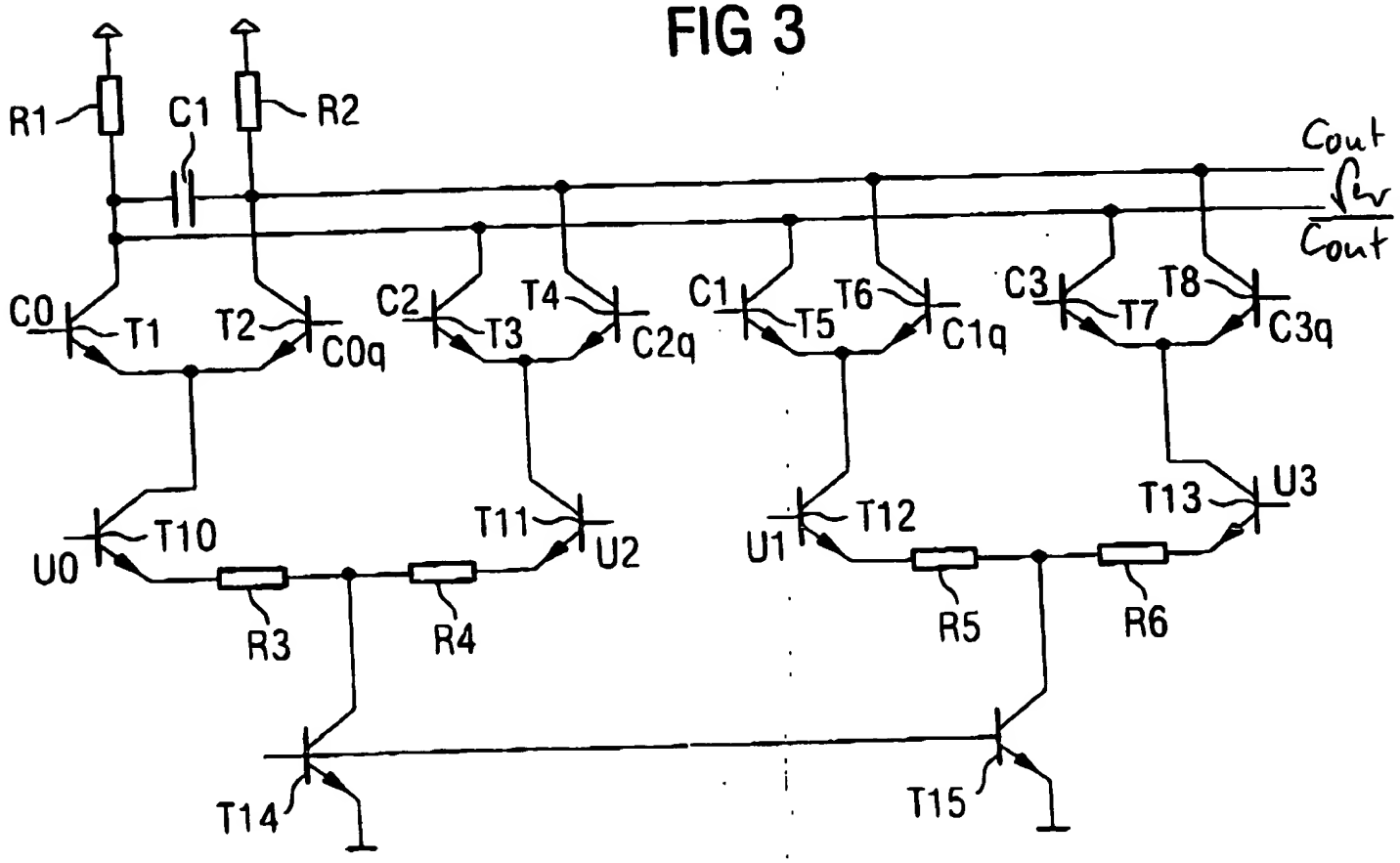

LOGIC UNIT
5
CIN
IIN
(C0 ... C3)
8
2
3
4
DATA SIGNAL
PHASE DETECTOR
CHARGE PUMP
Ucp
PHASE SHIFTER
Cout
1

FIG 3


R1
C1
R2
Cout
Cout
C0
T1
T2
C0q
C2
T3
T4
C2q
C1
T5
T6
C1q
C3
T7
T8
C3q
T10
U0
T11
U2
T12
U1
T13
U3
R3
R4
R5
R6
T14
T15

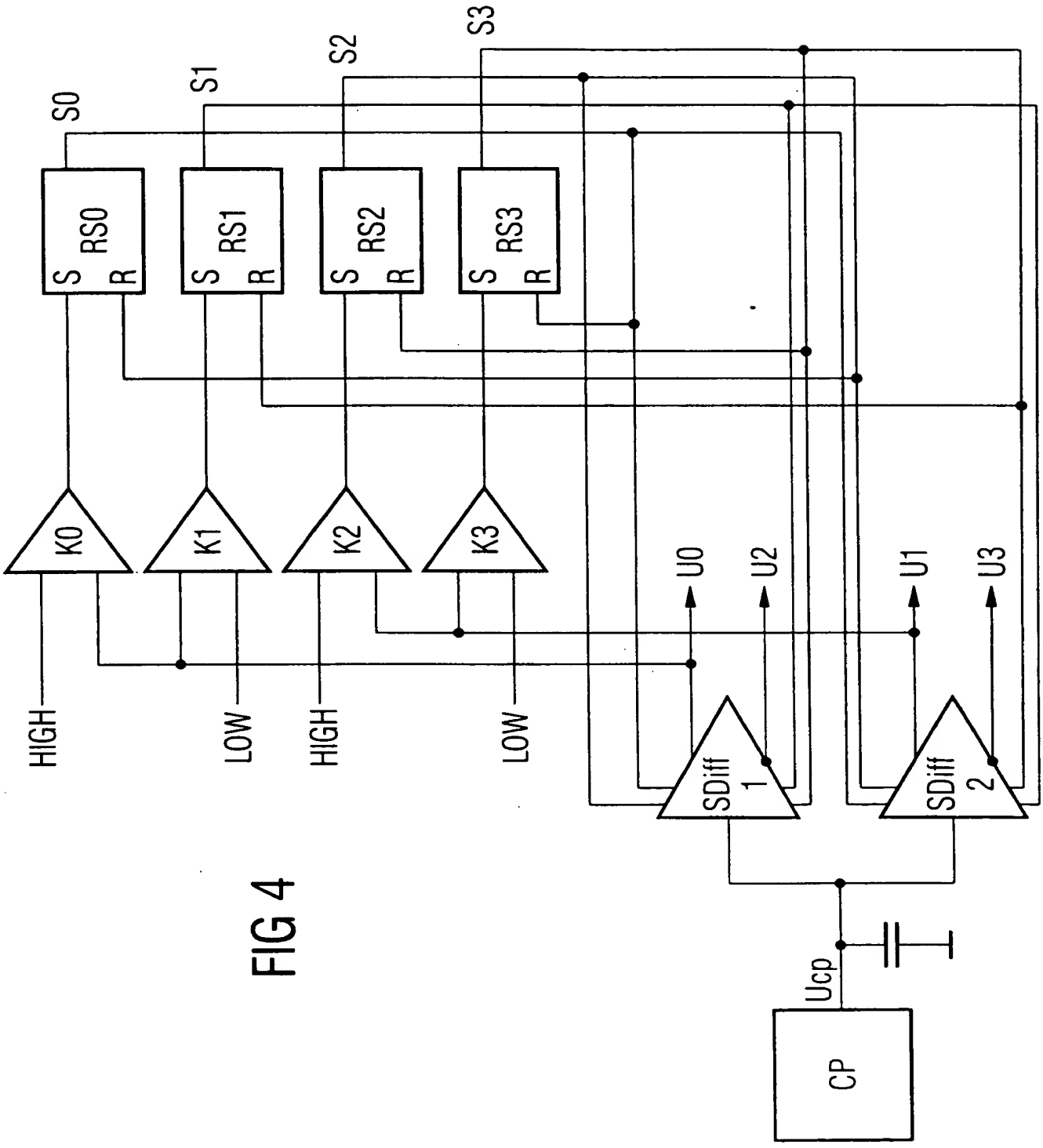

S0
S1
S2
S3
S
RS0
R
S
RS1
R
S
RS2
R
S
RS3
R
K0
K1
K2
K3
HIGH
LOW
HIGH
LOW
U0
U2
U1
U3
SDiff
1
SDiff
2
Ucp
CP

FIG 4

FIG 5

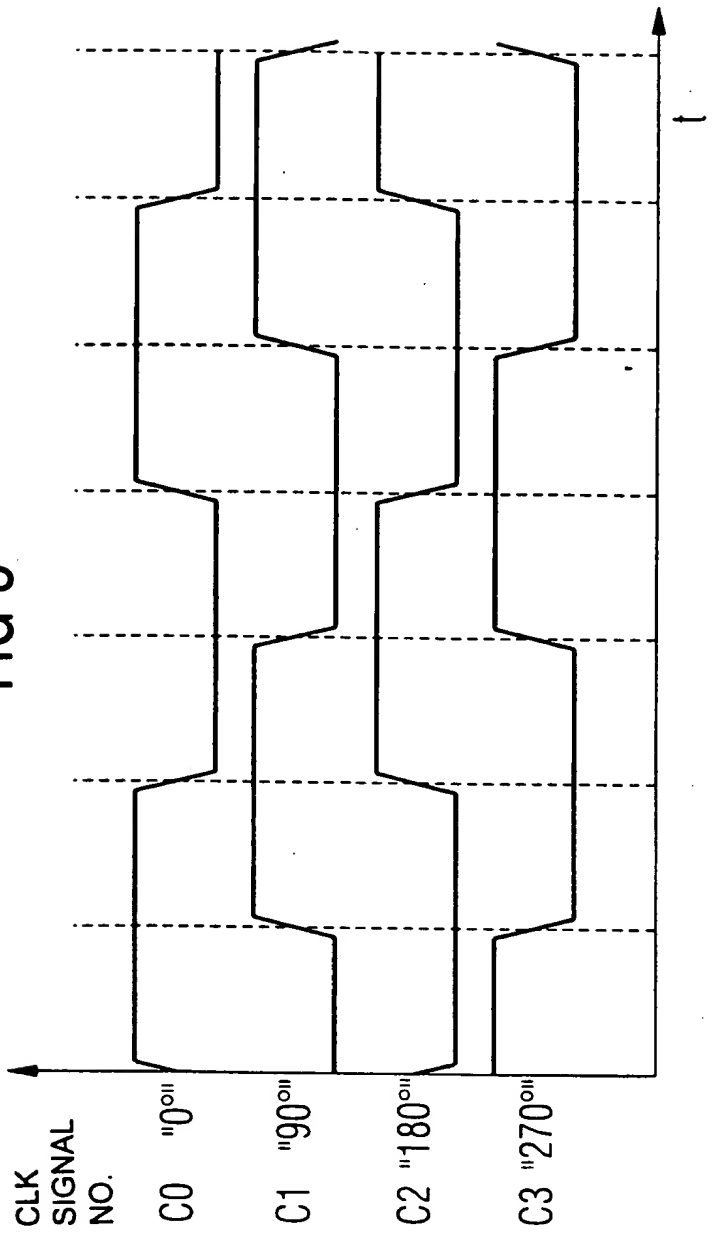


FIG 6

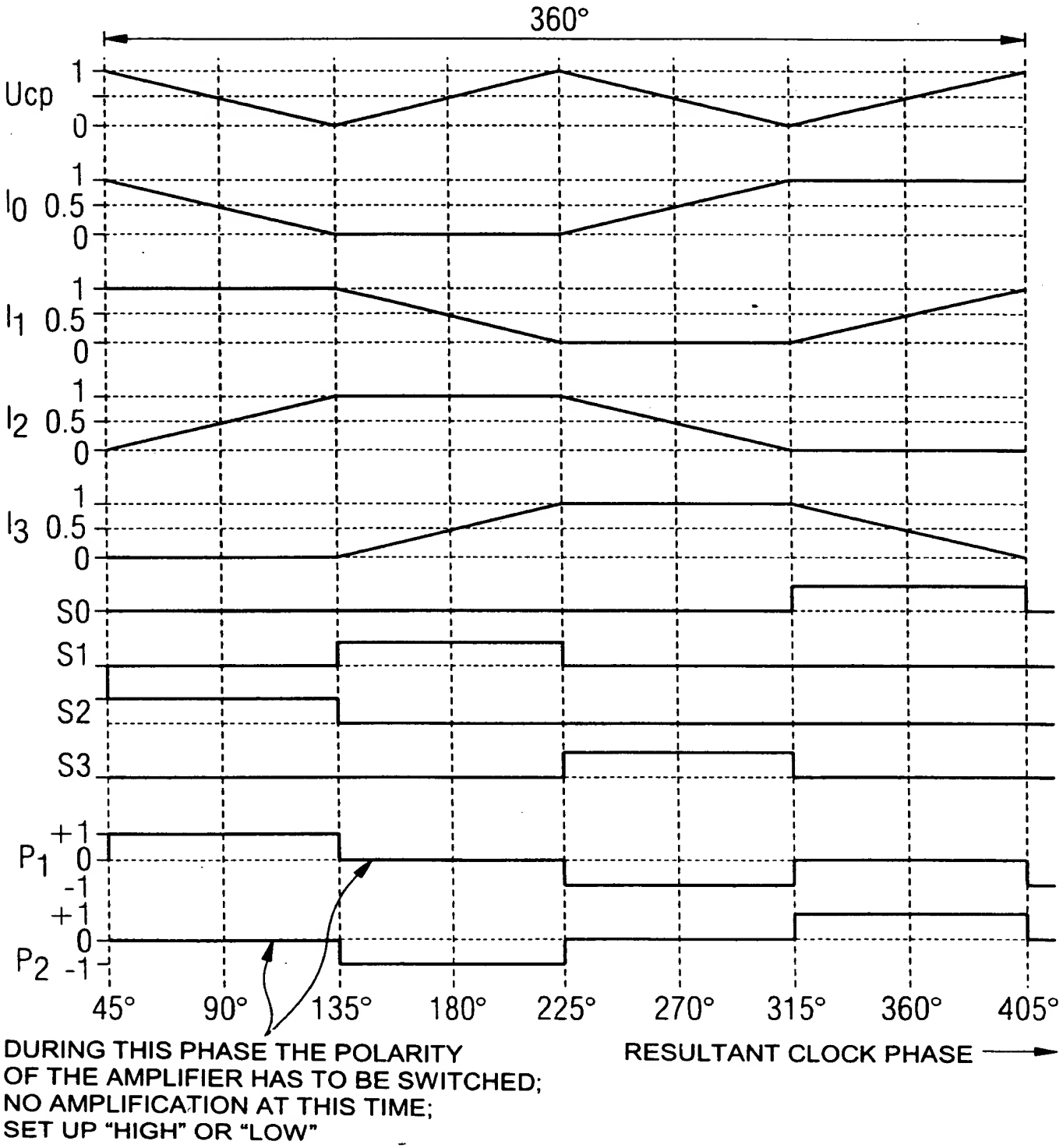

360°
Ucp
1
0
I0 0.5
I1 0.5
I2 0.5
I3 0.5
S0
S1
S2
S3
P1
+1
0
-1
P2
45°
90°
135°
180°
225°
270°
315°
360°
405°
DURING THIS PHASE THE POLARITY
OF THE AMPLIFIER HAS TO BE SWITCHED;
NO AMPLIFICATION AT THIS TIME;
SET UP "HIGH" OR "LOW"
RESULTANT CLOCK PHASE

FIG 7

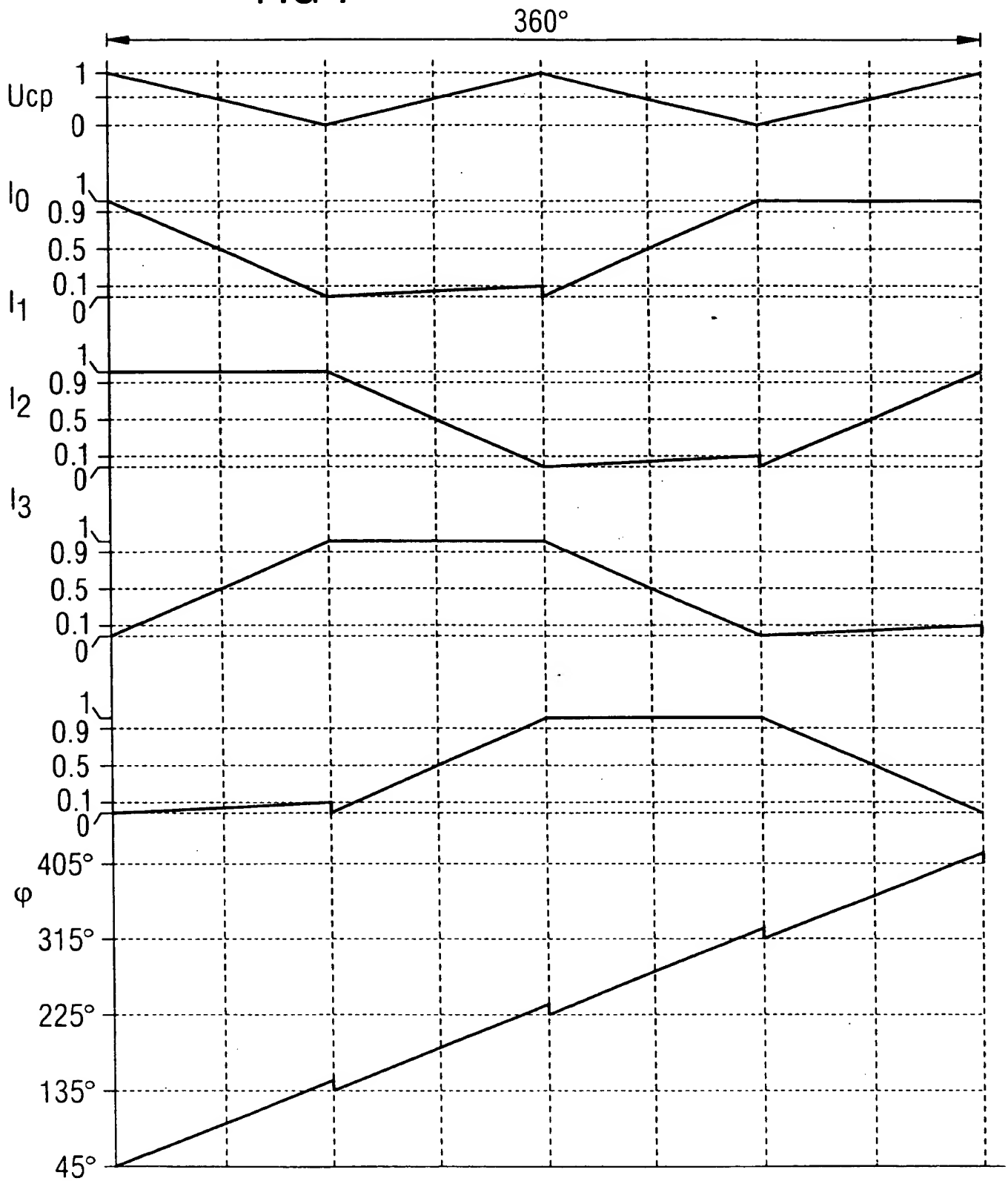

360°
Ucp
1
0
I0
1
0.9
0.5
0.1
0
I1
1
0.9
0.5
0.1
0
I2
1
0.9
0.5
0.1
0
I3
1
0.9
0.5
0.1
0
φ
405°
315°
225°
135°
45°

FIG 8

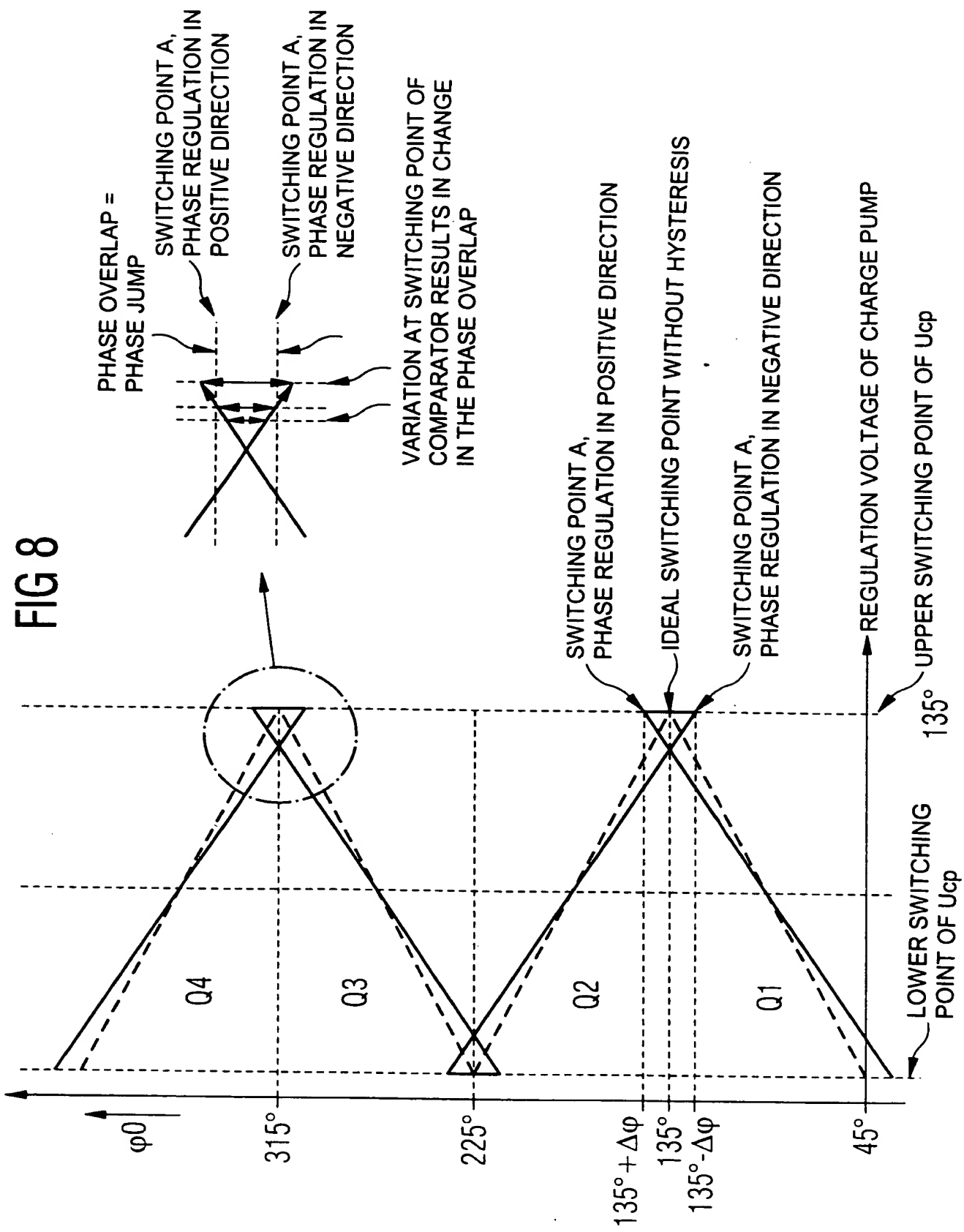

PHASE OVERLAP = PHASE JUMP
SWITCHING POINT A, PHASE REGULATION IN POSITIVE DIRECTION
SWITCHING POINT A, PHASE REGULATION IN NEGATIVE DIRECTION
VARIATION AT SWITCHING POINT OF COMPARATOR RESULTS IN CHANGE IN THE PHASE OVERLAP
SWITCHING POINT A, PHASE REGULATION IN POSITIVE DIRECTION
IDEAL SWITCHING POINT WITHOUT HYSTERESIS
SWITCHING POINT A, PHASE REGULATION IN NEGATIVE DIRECTION
REGULATION VOLTAGE OF CHARGE PUMP
UPPER SWITCHING POINT OF Ucp
LOWER SWITCHING POINT OF Ucp
Q4
Q3
Q2
Q1
φ0
315°
225°
135°+Δφ
135°
135°-Δφ
45°
135°

FIG 9

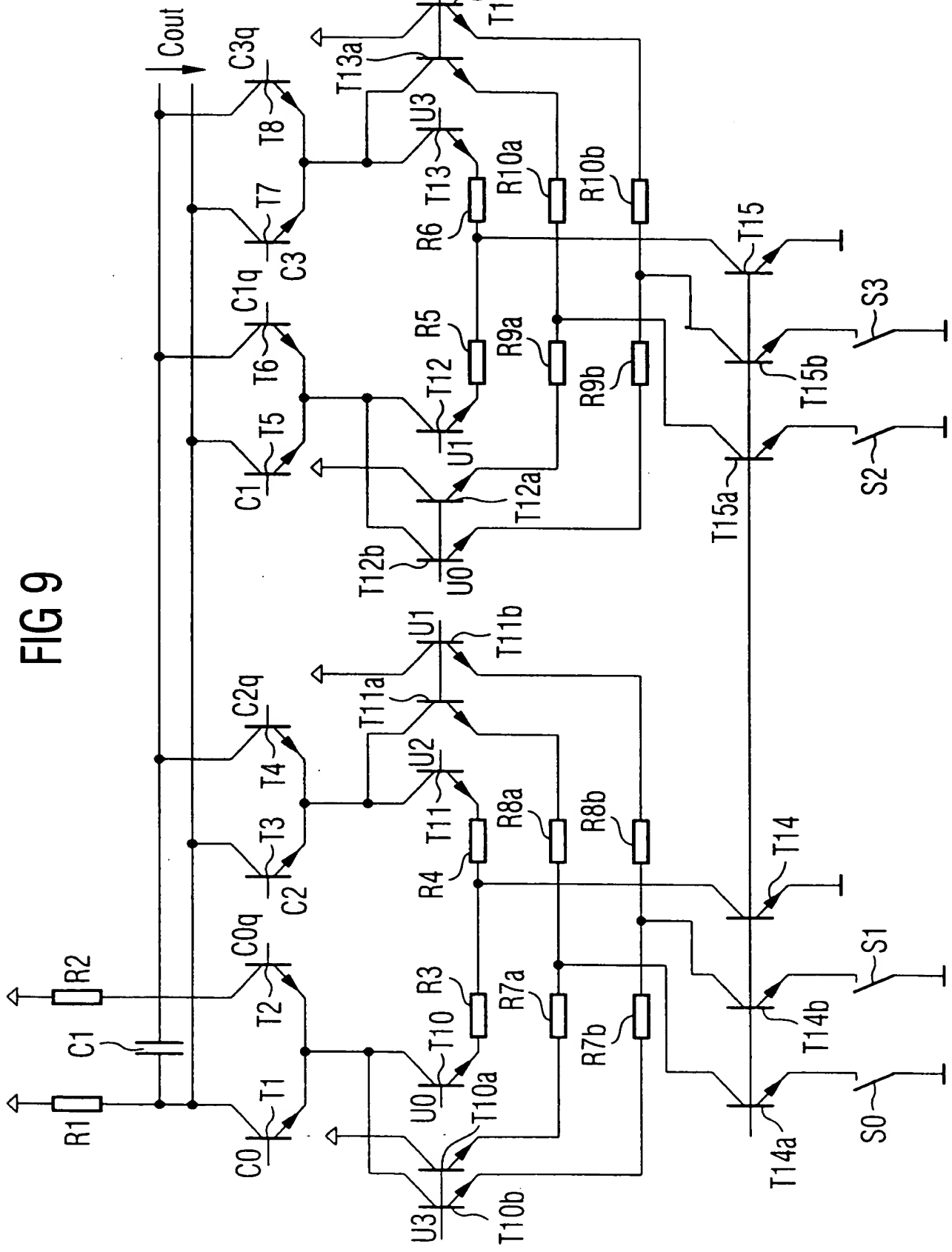

Cout
C3q
C1q
C2q
C0q
C3
C2
C1
C0
T8
T7
T6
T5
T4
T3
T2
T1
R1
R2
C1
U3
U2
U1
U0
T13a
T13b
T13
T12a
T12b
T12
T11a
T11b
T11
T10a
T10b
T10
R6
R5
R4
R3
R10a
R10b
R9a
R9b
R8a
R8b
R7a
R7b
T15
T15a
T15b
T14
T14a
T14b
S3
S2
S1
S0

FIG 10

	45°-135°	135°-225°	225°-315°	315°-405°
S0	0	0	0	1
S1	0	1	0	0
S2	1	0	0	0
S3	0	0	1	0
U0 (POSITIVE OUTPUT FROM SDiff1)	POSITIVE	low	NEGATIVE	high
U1 (POSITIVE OUTPUT FROM SDiff2)	high	NEGATIVE	low	POSITIVE
U2 (NEGATIVE OUTPUT FROM SDiff1)	NEGATIVE	high	POSITIVE	low
U3 (NEGATIVE OUTPUT FROM SDiff2)	low	POSITIVE	high	NEGATIVE
G1 (GAIN OF SDiff1)	+1	0	-1	0
G2 (GAIN OF SDiff2)	0	-1	0	+1